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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/804,699	03/19/2004	Tim J. Bales	DB001094-000	9148

57694 7590 02/26/2007

JONES DAY
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EXAMINER	
CHANG, DANIEL D	
ART UNIT	**PAPER NUMBER**
2819	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/26/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/804,699	BALES, TIM J.	
	Examiner	Art Unit	
	Daniel D. Chang	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4,5,7-9,11,13-15,17-45,64 and 65* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *20-31* is/are allowed.

6)☒ Claim(s) *1,7,32,33,37,64 and 65* is/are rejected.

7)☒ Claim(s) *2,4,5,8,9,11,13-15,17-19,34-36 and 38-45* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on January 11, 2007 has been entered.

Claim Objections

Claim 65 is objected to because of the following informalities: Lines 18-19, the clause, "and to have an increased output impedance when output impedance of said first MOS transistor decreases" is redundant, therefore, it is suggested that on line 18, the wording, "increased output" be changed to "decreased output" and on line 19, the word, "decreases" after "first MOS transistor" be changed to "increases". Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 7, 32, 33, 37, 64, and 65 are rejected under 35 U.S.C. 102(b) as being anticipated by Fifield et al. (US 6,577,154 B2, hereinafter, "Fifield").

Regarding claim 32, Fifield discloses, in Fig. 2, a MOS driver circuit comprising:

a first MOS transistor (lower transistor in 40) configured to receive a controlled voltage (In) at a first input terminal (gate) thereof; and

a second MOS transistor (Output Device in 30) coupled to said first MOS transistor and configured to receive a differential voltage (gatenmim via 40) at a second input terminal (gate) thereof,

wherein said second MOS transistor is configured to have an increased output impedance (when predrive stage portion switches GATEN of the output stage 30 to ground; see paragraph 0038) when output impedance of said first MOS transistor decreases (when lower transistor in 40 turns ON), and to have a decreased output impedance (when predrive stage portion switches GATEN of the output stage 30 to GATENMIM; see paragraph 0038) when output impedance of said first MOS transistor increases (when lower transistor in 40 turns OFF) so as to maintain an output impedance of said MOS driver circuit (DQ) within a desired tolerance (see paragraph 0041).

Regarding claim 33, Fifield discloses, in Fig. 2, that wherein said first and said second input terminals are respective gate terminals of said first and said second MOS transistors (see gates of lower transistor in 40 and Output Device in 30).

Regarding claim 37, Fifield discloses, in Fig. 2, a MOS driver circuit comprising:

a first MOS transistor (Sample Output Device in 70) configured to receive a controlled voltage (gatenmim) at a first input terminal (gate) thereof; and

a second MOS transistor (Output Device in 30) coupled (via Pre Drive 40) to said first MOS transistor and configured to receive a differential voltage (gatenmim via Pre Drive 40) at a second input terminal (gate) thereof;

wherein said second MOS transistor (Output Device in 30) is configured to compensate for changes in output impedance of said first MOS transistor (Sample Output Device in 70) through corresponding changes in output impedance of said second MOS transistor so as to maintain an output impedance of said MOS driver circuit (DQ) within a desired tolerance (see paragraph 0041).

Claims 1, 7, 64, and 65 are essentially the same in scope as claims 32 and 37, and are rejected similarly.

Regarding claims 64 and 65, as for the limitation, a processor, memory controller, memory device, first bus and second bus, input device, output device, and data storage device, it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex parte Masham, 2 USPQ2d 1647 (1987).

Response to Arguments

Applicant's arguments with respect to claims 1, 2, 4, 5, 7, 8, 20, 26, 32-34, 37, 38, 64, and 65 have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

Claims 20-31 are allowable.

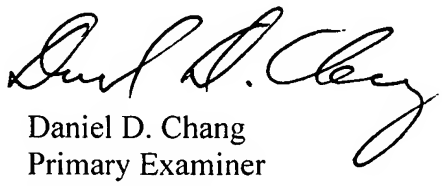
Claims, 2, 4, 5, 8, 9, 11, 13-15, 17-19, 34-36, and 38-45 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel D. Chang whose telephone number is (571) 272-1801. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Daniel D. Chang
Primary Examiner
Art Unit 2819

dc

DANIEL CHANG
PRIMARY EXAMINER